sequence, and to create electrical analysis output files;

an integrator, coupled to said analysis generator, operable to integrate said analysis output files in controlled sequence into a single model file, to quantify alternative choices, and to store said file in a report storage; and

an output generator, coupled to said integrator, operable to create summary files in specific formats or displays.

Claim 2, line 4, after "select" insert – leadframe --;

line 5, delete "structure" and insert – package --.

Add the following new claims:

32. A system as in claim 1 wherein said segment selector is operable to define a set of continuous conductor subdivisions.

33. A system as in claim 32 wherein said sequence organizer is operable to define said subdivisions starting from the chip side of the package.

Remarks

Favorable reconsideration and allowance of the application are respectfully requested in view of the above amendments and the following comments.

The rejection of all claims under 35 USC 112, as failing to comply with the enablement requirement, is respectfully traversed. The specification is clearly adequate to enable one skilled in the art to implement the **analysis generator** portion of the invention, without undue experimentation. For example, the work done at the University of Arizona at Tucson is well-known, as published by Michael R. Scheinfein et al, "Electrical Performance of High-Speed Interconnect Systems," IEEE Transactions on Components, Hybrids, and Manufacturing Technology, vol CHMT-10, No. 3, p. 303-309, September 1987 (copy enclosed).

Also enclosed are the following two articles, showing other examples of how to structure an analysis generator, useful in the context of applicant's invention: